FIG. 1

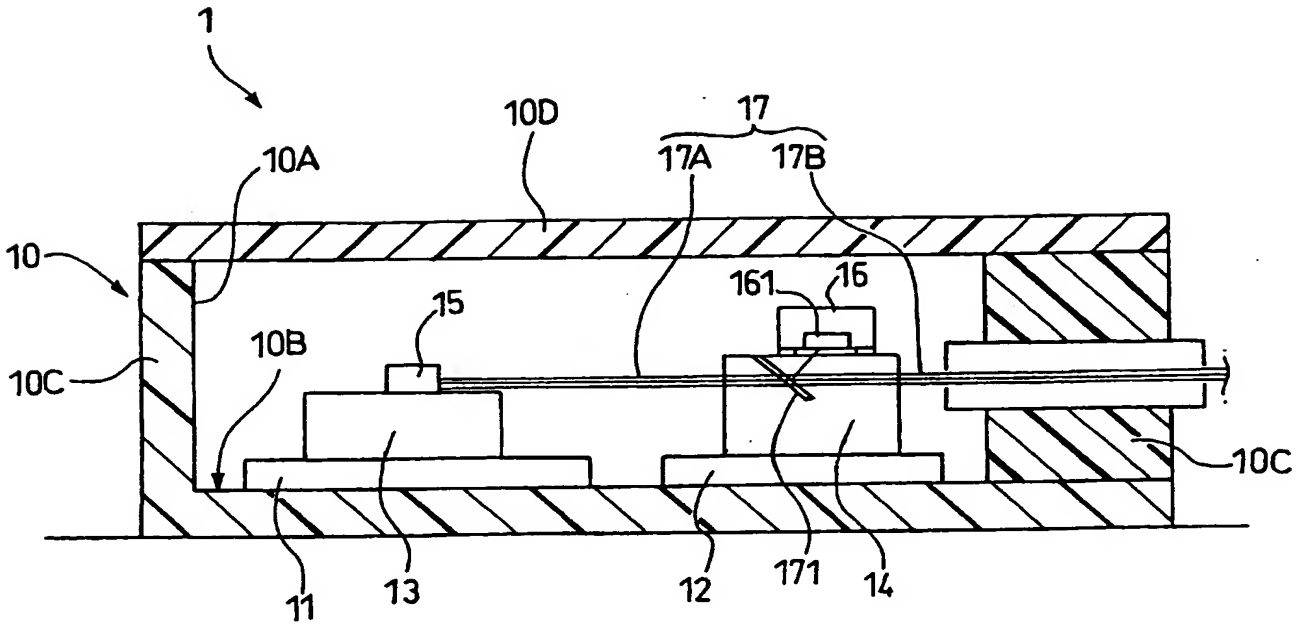


FIG. 2

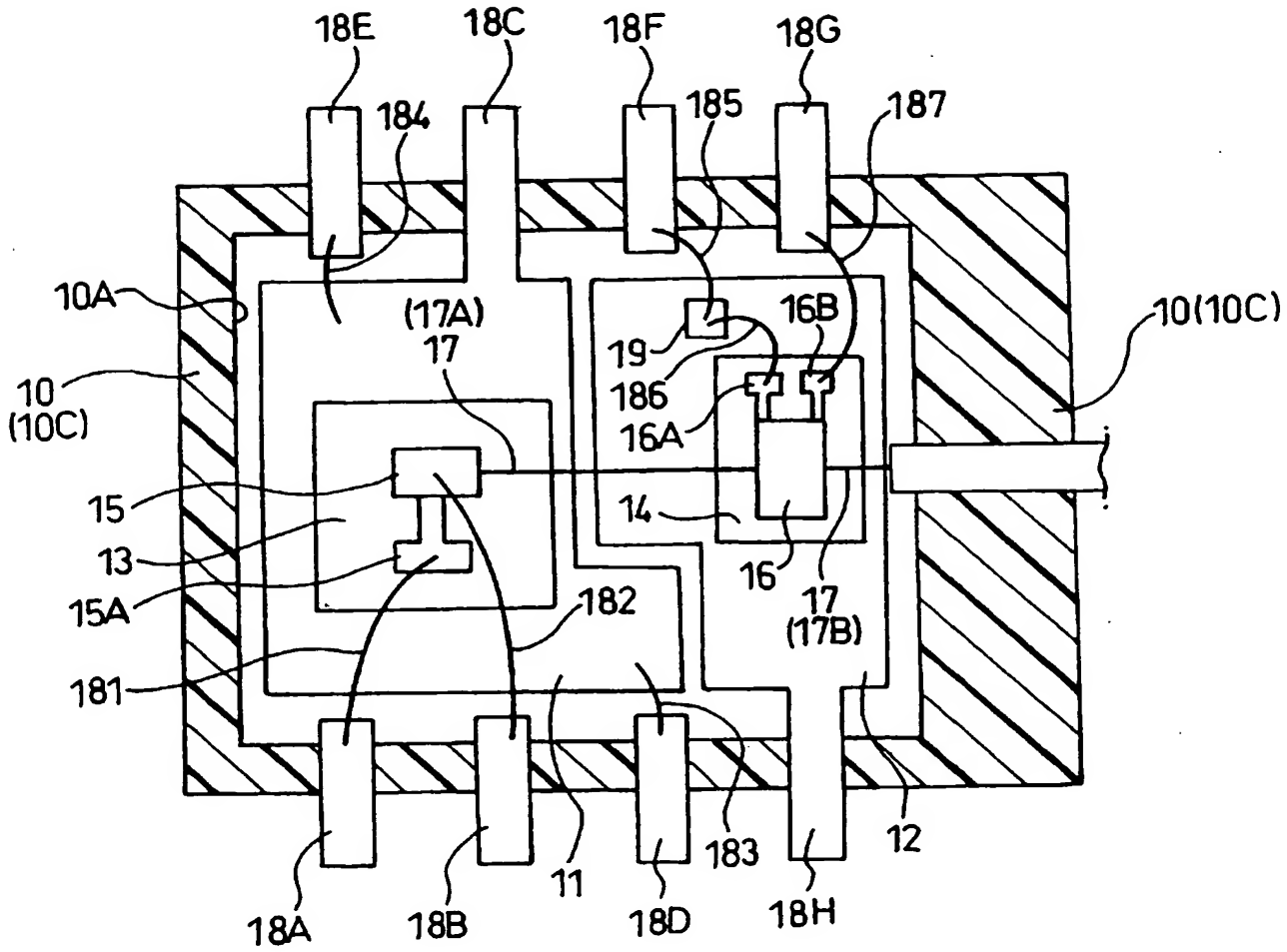

18E
18C
18F
18G
184
185
187
10A
(17A)
17
19
16B
10(10C)
10
(10C)
186
16A
15
14
13
16
15A
182
17
(17B)
181
183
12
11
18A
18B
18D
18H

FIG. 3 (C)

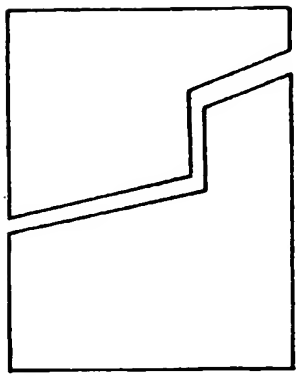


FIG. 3 (B)

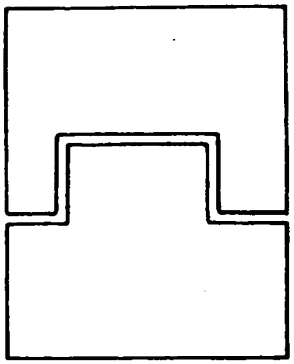


FIG. 3 (E)

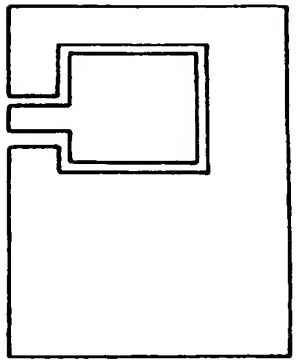


FIG. 3 (A)

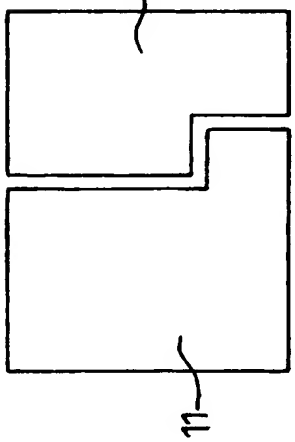


FIG. 3 (D)

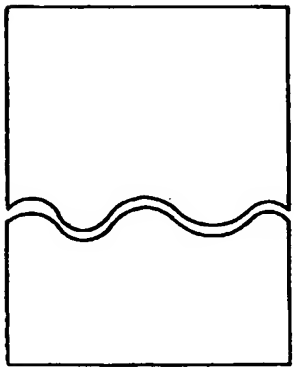


FIG. 4

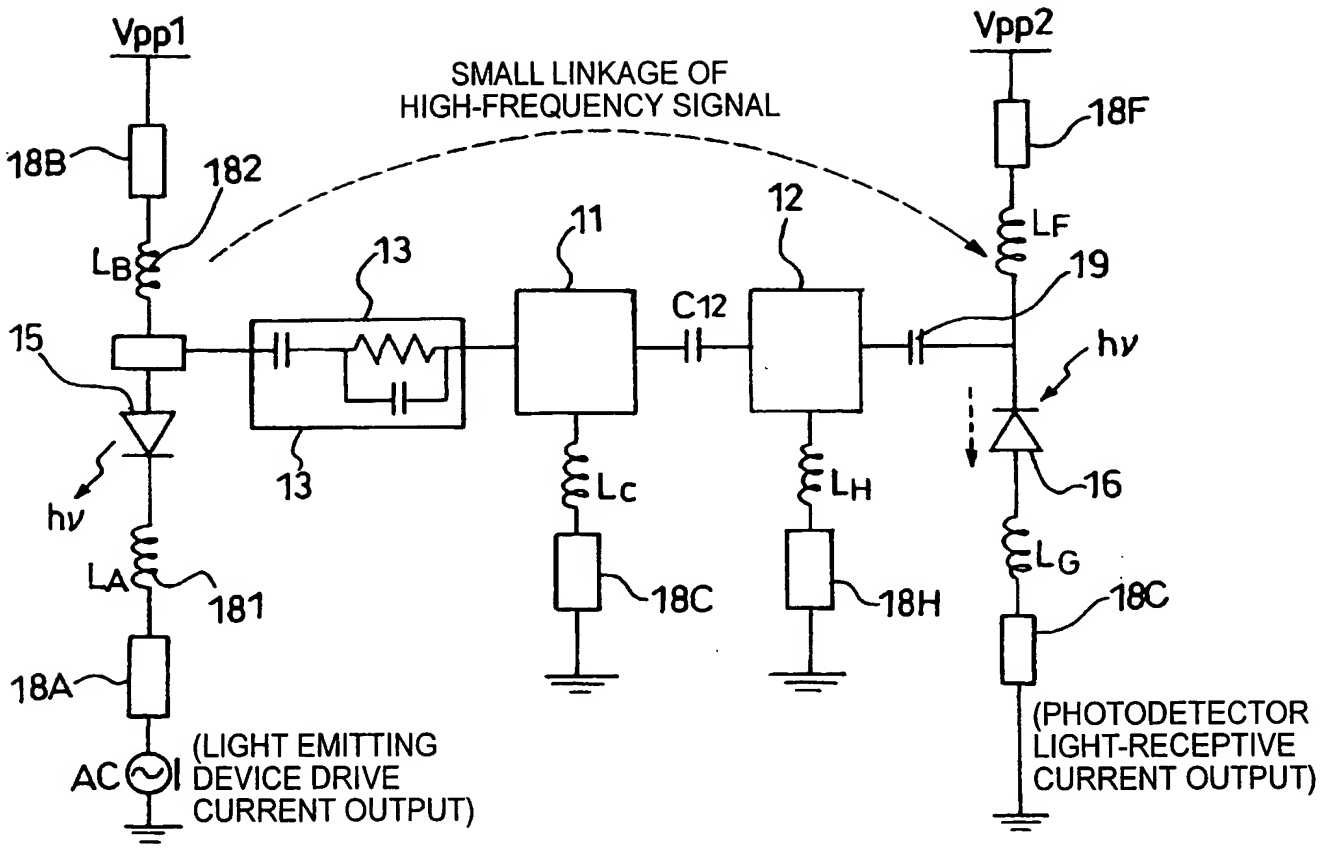

Vpp1
Vpp2
SMALL LINKAGE OF
HIGH-FREQUENCY SIGNAL
18B
182
18F
LB
LF
13
11
12
19
15
C12
hν
13
Lc
LH
16
hν
LA
181
LG
18C
18H
18C
18A
AC
(LIGHT EMITTING
DEVICE DRIVE
CURRENT OUTPUT)
(PHOTODETECTOR
LIGHT-RECEPTIVE
CURRENT OUTPUT)

FIG. 5

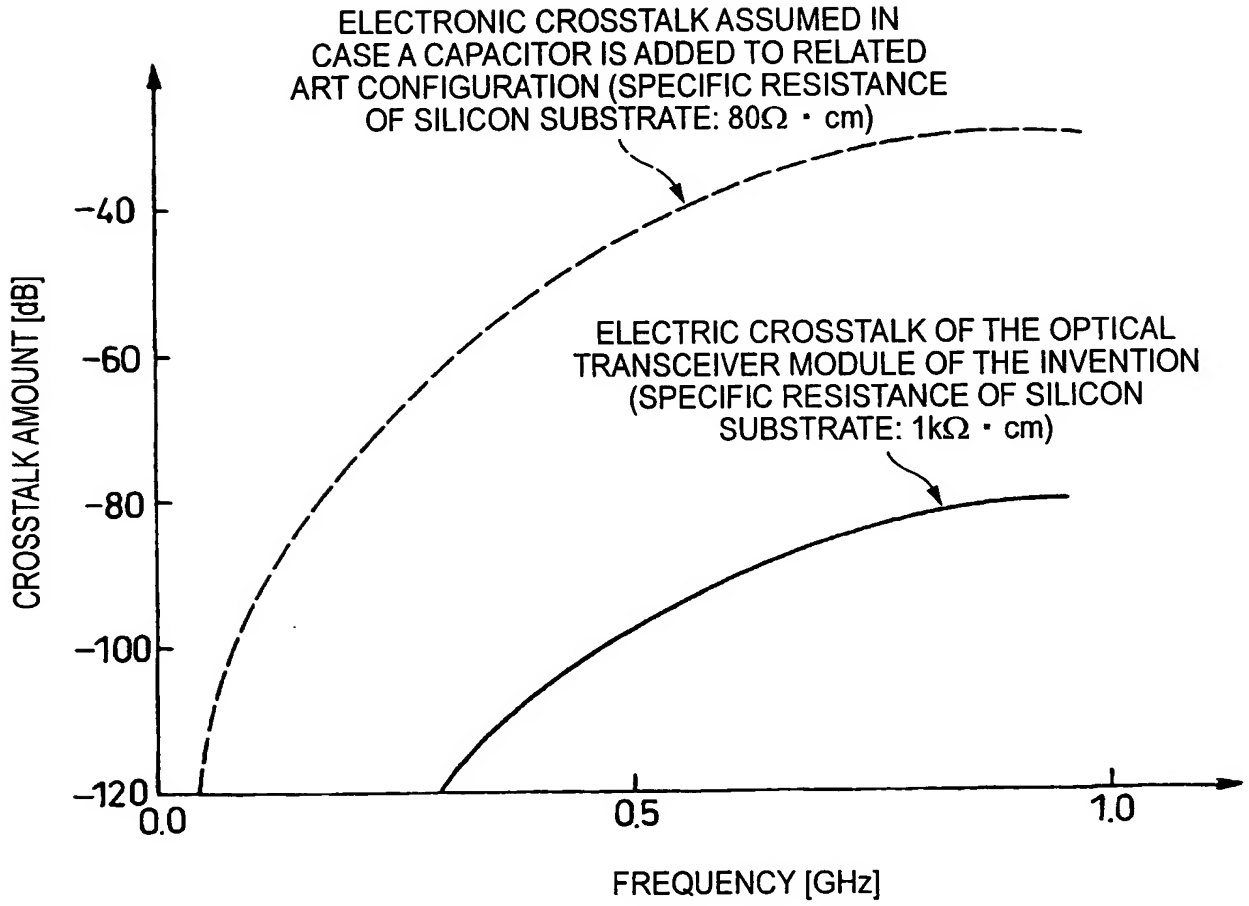

ELECTRONIC CROSSTALK ASSUMED IN CASE A CAPACITOR IS ADDED TO RELATED ART CONFIGURATION (SPECIFIC RESISTANCE OF SILICON SUBSTRATE: 80Ω · cm)
ELECTRIC CROSSTALK OF THE OPTICAL TRANSCEIVER MODULE OF THE INVENTION (SPECIFIC RESISTANCE OF SILICON SUBSTRATE: 1kΩ · cm)
CROSSTALK AMOUNT [dB]
-40
-60
-80
-100
-120
0.0
0.5
1.0
FREQUENCY [GHz]

FIG. 6

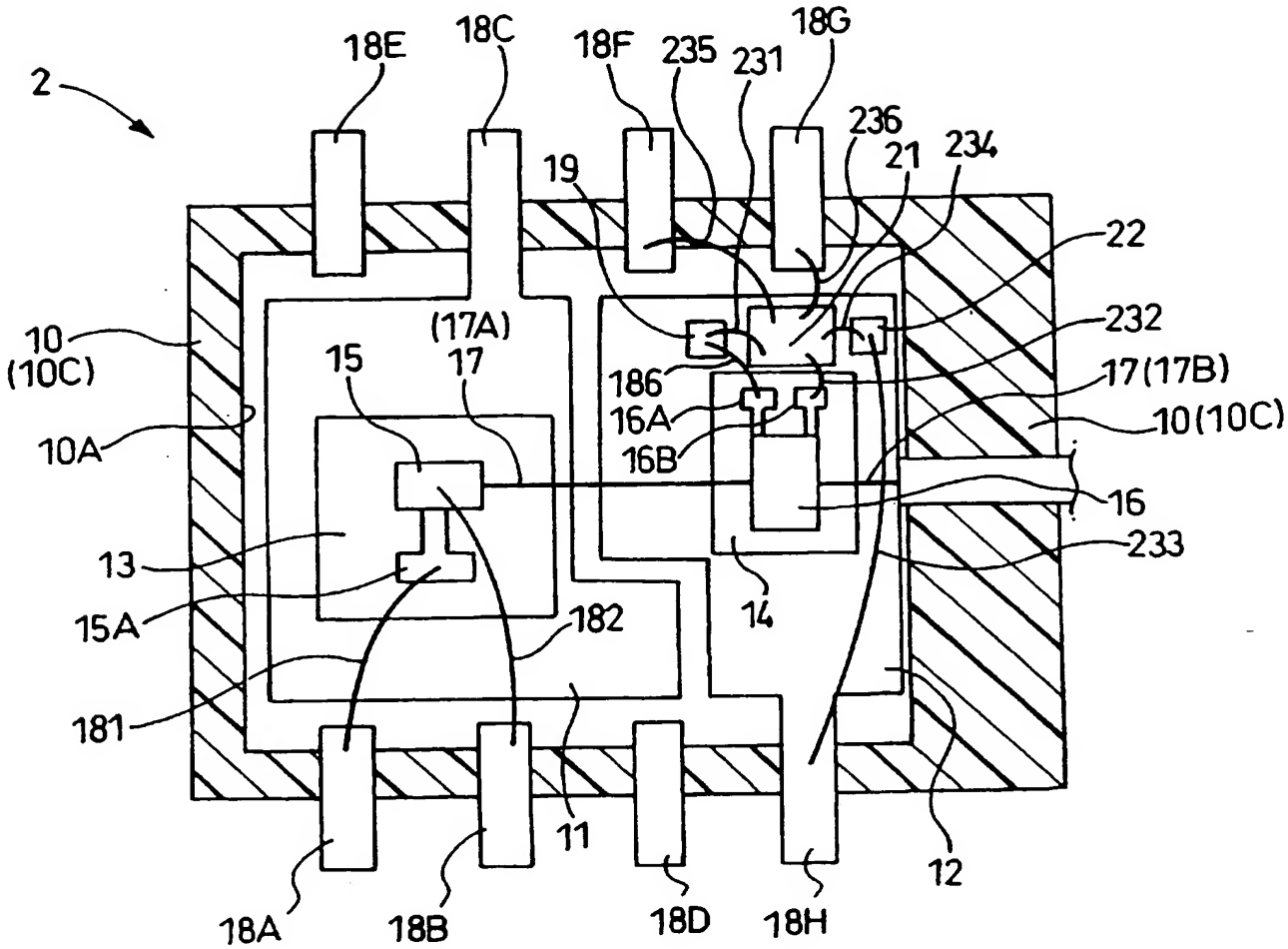

2
18E
18C
18F
235
231
18G
236
21
234
19
22
232
17(17B)
10(10C)
16
233
10
(10C)
10A
(17A)
17
15
186
16A
16B
13
15A
182
14
181
11
12
18A
18B
18D
18H

FIG. 7

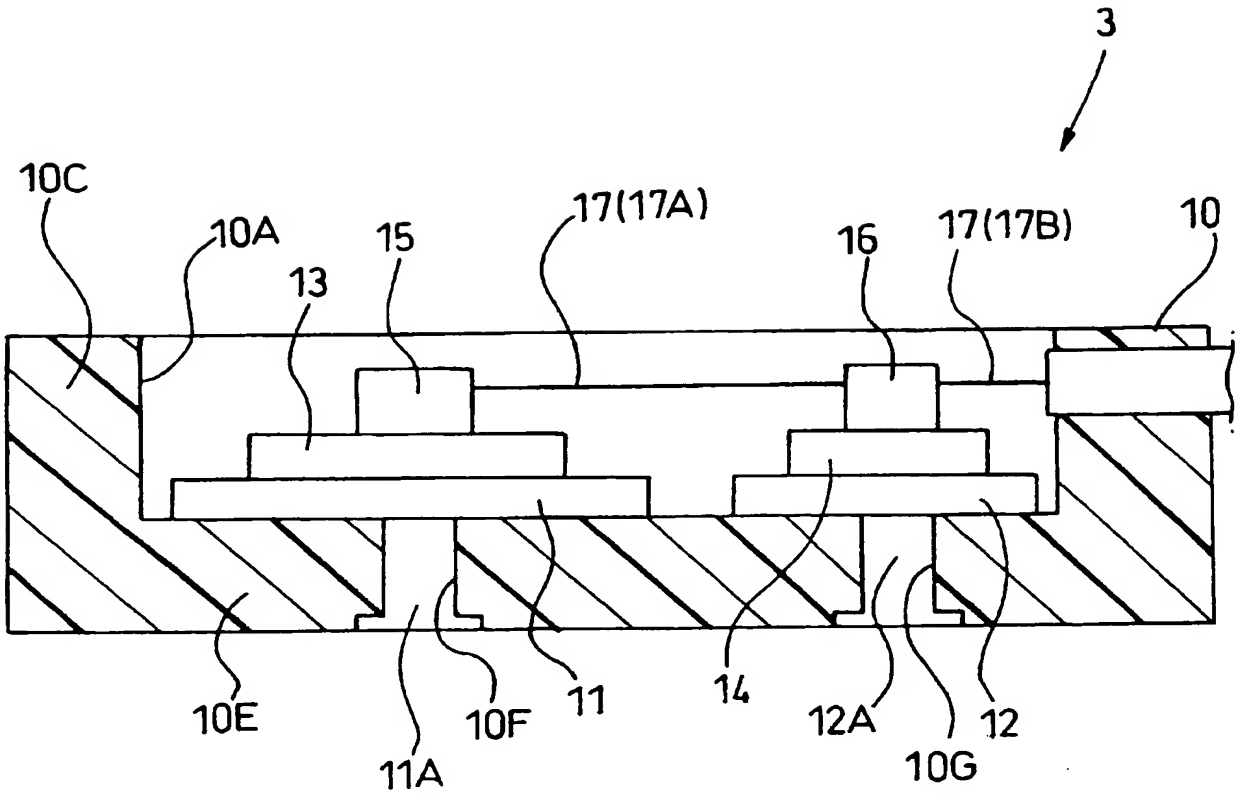


FIG. 8

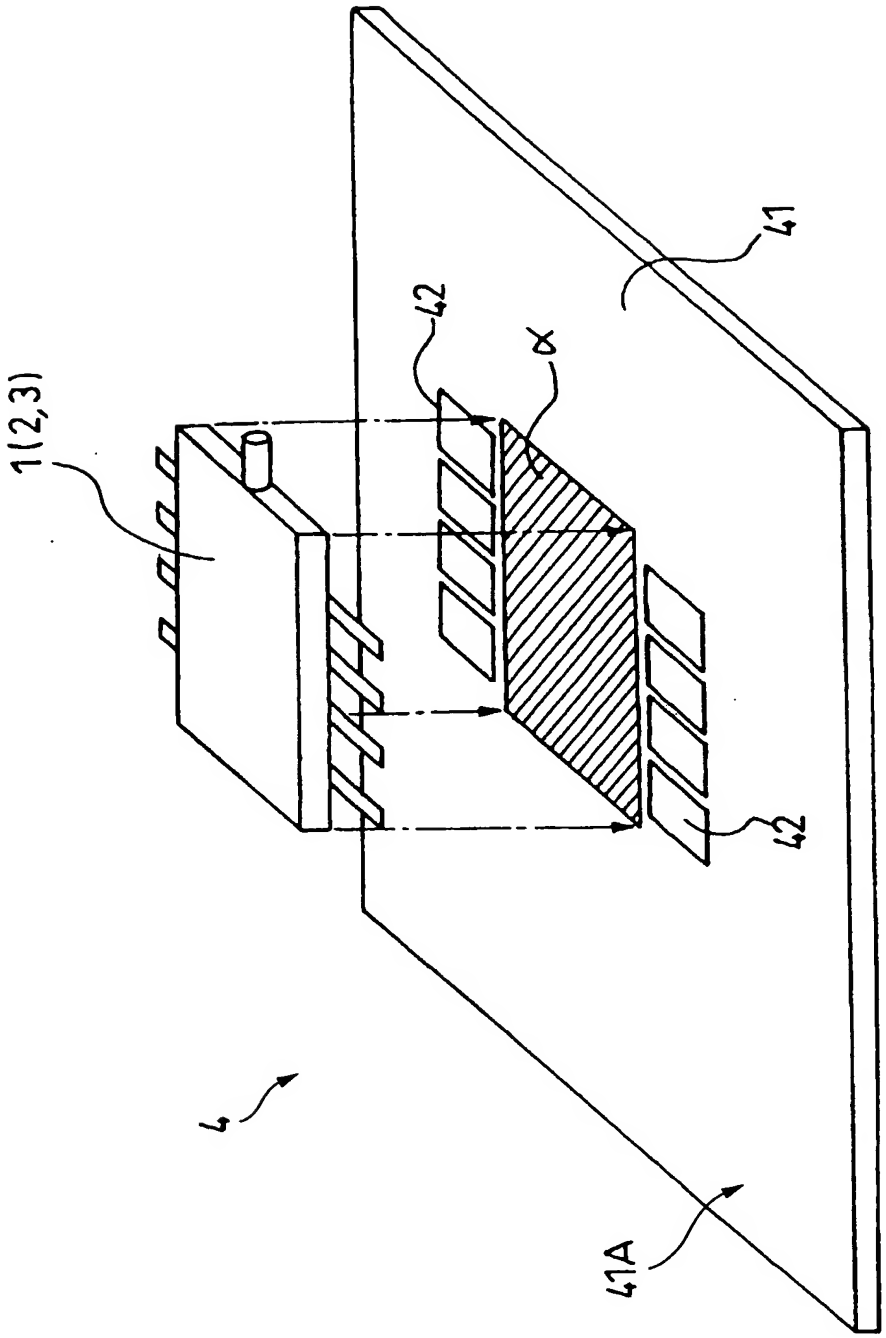


FIG. 9

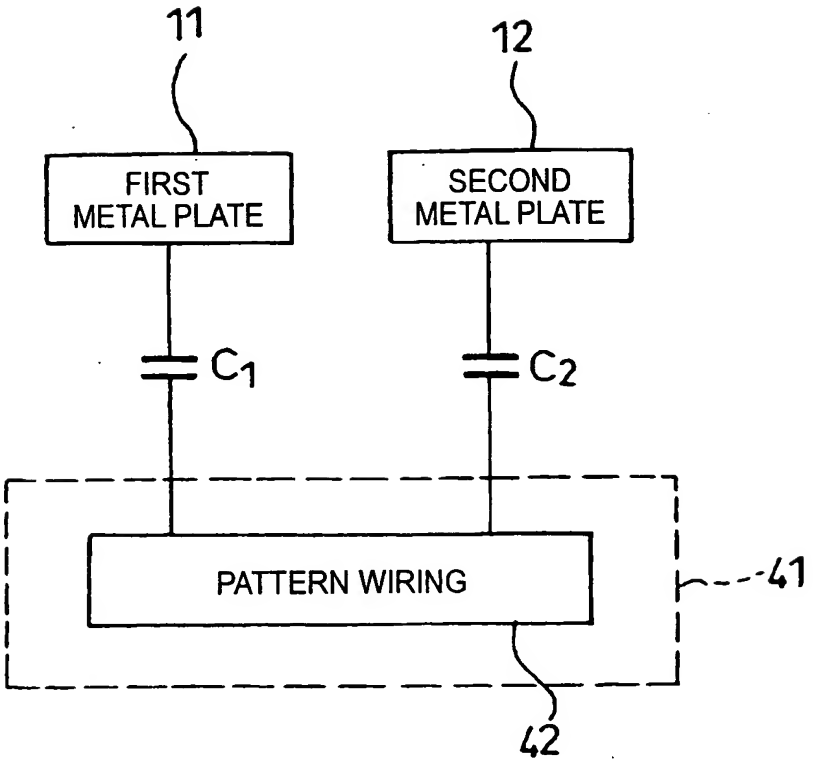
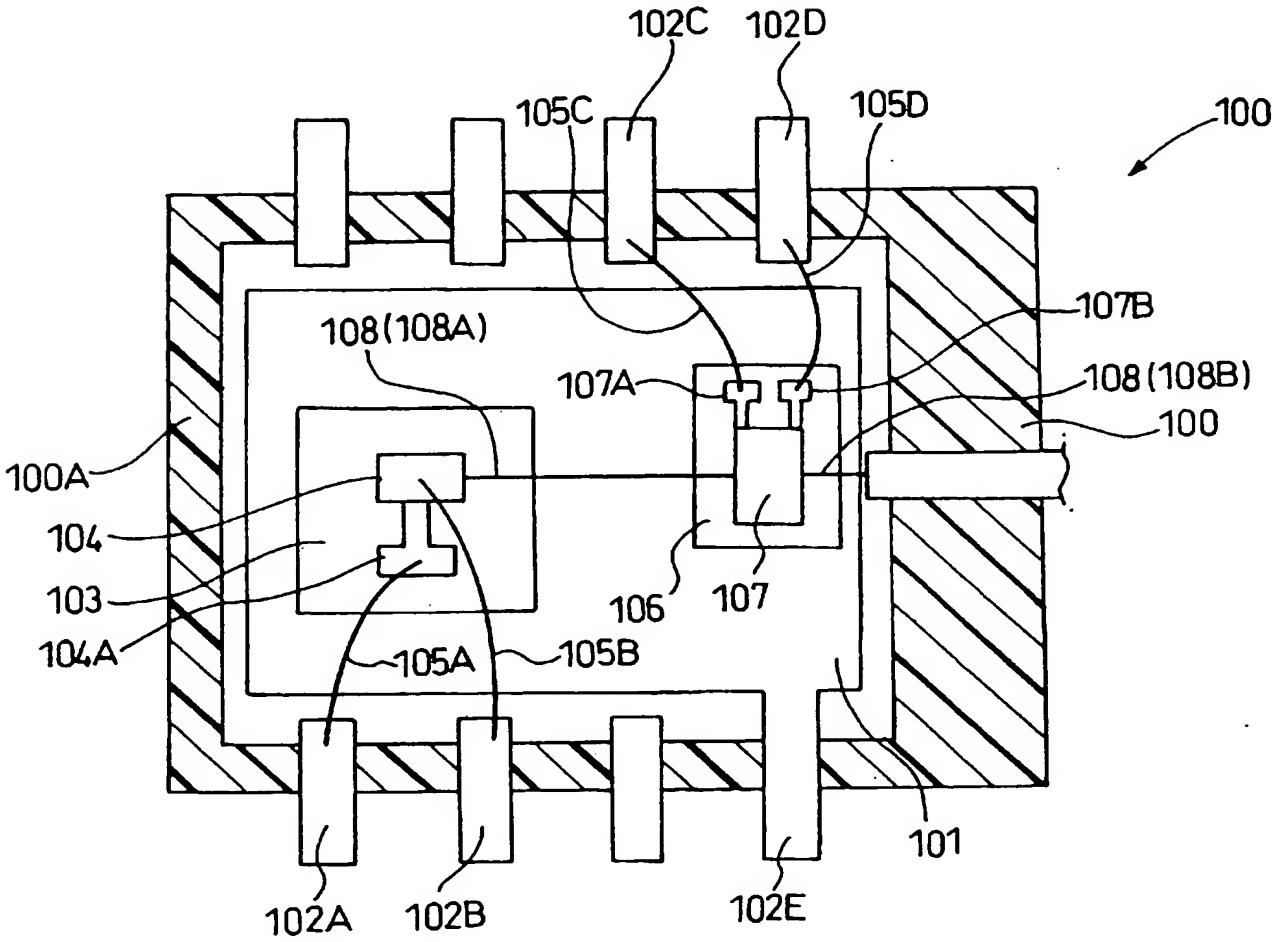

11
12
FIRST METAL PLATE
SECOND METAL PLATE
C1
C2
PATTERN WIRING
41
42

FIG. 10


102C
102D
105C
105D
100
107B
108(108A)
107A
108(108B)
100
100A
104
103
104A
106
107
105A
105B
101
102A
102B
102E

Customer No.: 52054
Application No.: TBD
Applicant: Kazuhiro Nojima et al.
Atty. Docket No.: 40062

FIG. 11